

IN THE CLAIMS

Please amend the claims as follows.

For the Examiner's convenience, a list of all claims is included below.

31. (Currently Amended) A printed circuit board (PCB) comprising:
 - a first signal routing layer formed on a first surface of the PCB;
 - an electrically conductive layer, ~~the electrically conductive layer comprising one of a conductive plane and a second signal routing layer;~~
 - at least one padless via extending from the first signal routing layer to the electrically conductive layer, the at least one padless via in electrical contact with the electrically conductive layer; and
 - a layer of solder mask material formed over the first signal routing layer, the layer of solder mask material having at least one opening to expose the at least one padless via.
32. (Previously presented) The PCB of claim 31, wherein the electrically conductive layer comprises the second signal routing layer and the at least one padless via is in electrical contact with a conductive trace on the second signal routing layer.
33. (Previously presented) The PCB of claim 31, further comprising a via plug formed within the padless via.

34. (Previously presented) The PCB of claim 33, wherein the via plug is formed of an electrically conductive material.

35. (Previously presented) The PCB of claim 31, further comprising a component attached to the PCB with a solder interconnection between a contact pad on a bottom surface of the component and the at least one padless via.

36. (Currently Amended) A printed circuit board (PCB) comprising:
a first signal routing layer formed on a first surface of the PCB;
at least one electrically conductive layer, ~~the at least one electrically conductive layer comprising one of conductive plane and a second signal routing layer~~; and
an array of interconnections formed on the first surface of the PCB, the array of interconnections including at least one padless via extending from the first signal routing layer to the at least one electrically conductive layer, wherein the padless via is in electrical contact with the at least electrically conductive layer.

37. (Previously presented) The PCB of claim 36, wherein the at least one electrically conductive layer comprises the second signal routing layer and the at least one padless via is in electrical contact with a conductive trace on the second signal routing layer.

38. (Previously presented) The PCB of claim 36, further comprising an electrically conductive via plug formed within the at least one padless via.

39. (Previously presented) The PCB of claim 36, wherein the array of interconnections further comprises at least one contact pad electrically coupled with a conductive trace on the first signal routing layer, wherein the at least one contact pad has a diameter less than 18 mils.

40. (Previously presented) The PCB of claim 36, wherein the at least one padless via has a diameter of 12 mils or less.

41. (Currently Amended) A system comprising:
a printed circuit board (PCB) including
a first signal routing layer formed on a first surface of the PCB,
at least one electrically conductive layer, ~~the at least one electrically conductive layer comprising one of a conductive plane and a second signal routing layer, and~~
~~the at least one electrically conductive layer comprising one of a conductive plane and a second signal routing layer, and~~
an array of interconnections formed on the first surface of the PCB,
wherein the array of interconnections includes at least one padless via extending from the first signal routing layer to the at least one electrically conductive layer, the at least one padless via electrically connected to the at least one electrically conductive layer; and
a component attached to the PCB by a plurality of solder ball interconnections between the array of interconnections formed on the first surface of the PCB and a

corresponding array of contact pads disposed on a bottom surface of the electronic component.

42. (Previously presented) The system of claim 41, wherein the at least one electrically conductive layer comprises the second signal routing layer and the at least one padless via is in electrical contact with a conductive trace on the second signal routing layer.

43. (Previously presented) The system of claim 41, further comprising at least two conductive traces on the first signal routing layer routed between the at least one padless via and an adjacent interconnection.

44. (Previously presented) The system of claim 43, wherein a width of the at least two conductive traces is approximately 3 mils.

45. (Previously presented) The system of claim 41, wherein the at least one padless via has a diameter of 12 mils or less.

46. (Previously presented) The system of claim 41, wherein the PCB is a motherboard and the component is a processor. 19.

47. (Currently Amended) A method of fabricating a printed circuit board (PCB) comprising:

forming a first signal routing layer on a first surface of a printed circuit board (PCB); and forming an array of interconnections on the first surface of the PCB, the array of interconnections comprising at least one padless via extending from the first signal routing layer to an electrically conductive layer, ~~the electrically conductive layer comprising one of a conductive plane and a second signal routing layer;~~ wherein the first padless via is in electrical contact with the electrically conductive layer.

48. (Previously presented) The method of claim 47, wherein the electrically conductive layer comprises the second signal routing layer and the at least one padless via is in electrical contact with a conductive trace on the second signal routing layer.

49. (Previously presented) The method of claim 47, wherein forming an array of interconnections on the first surface of the PCB comprises forming an array of interconnections having an array pitch of 0.8 mm or less.

50. (Previously presented) The method of claim 49, further comprising routing at least two conductive traces on the first signal routing layer between the at least one padless via and an adjacent interconnection.

51. (Previously presented) The method of claim 47, further comprising forming a via plug within the at least one padless via.

52. (Previously presented) The method of claim 51, wherein forming a via plug within the at least one padless via comprises overplating the at least one padless via to form a via plug of plating material.

53. (Previously presented) The method of claim 47, wherein forming an array of interconnections on the first surface of the PCB comprises forming at least one contact pad on the first surface of the PCB adjacent to the at least one padless via, the at least one contact pad in electrical contact with a conductive trace on the first signal routing layer.

54. (Currently Amended) A method of attaching a component to a printed circuit board (PCB) comprising:

aligning solder balls attached to an array of contact pads on a bottom surface of the component with a corresponding array of interconnections formed on a first surface of the PCB, the array of interconnections comprising at least one padless via extending from a first signal routing layer on the first surface of the PCB to an electrically conductive layer, ~~the electrically conductive layer comprising one of a conductive plane and a second signal routing layer within the PCB~~, wherein the at least one padless via is in electrical contact with the electrically conductive layer;

and

reflowing the solder balls to electrically connect the array of contact pads to the corresponding array of interconnections.

55. (Previously presented) The method of claim 54, wherein the electrically conductive layer comprises the second signal routing layer and the at least one padless via is in electrical contact with a conductive trace on the second signal routing layer.

56. (Previously presented) The method of claim 54, wherein the component is an electronic component housed in a ball grid array (BGA) package having a BGA pitch of 0.8 mm or less.

57. (Currently Amended) The method of claim 54[6], wherein the component is a land grid array (LGA) socket.

58. (New) The PCB of claim 31, wherein the electrically conductive layer comprises a conductive plane, and the at least one padless via is in electrical contact with the conductive plane.

59. (New) The PCB of claim 36, wherein the electrically conductive layer comprises a conductive plane, and the at least one padless via is in electrical contact with the conductive plane.

60. (New) The system of claim 41, wherein the electrically conductive layer comprises a conductive plane, and the at least one padless via is in electrical contact with the conductive plane.

61. (New) The method of claim 47, wherein the electrically conductive layer comprises a conductive plane, and the at least one padless via is in electrical contact with the conductive plane.

62. (New) The method of claim 54, wherein the electrically conductive layer comprises a conductive plane and the at least one padless via is in electrical contact with the conductive plane.